Comparative Study of Different Modulation Technique in Chaotic Communication

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Abstract

This is age of digital processing technique in which we trying to get high data rate and reducing the interferences. Chaotic communication is latest research area in communication. There is different modulation technique implemented in it DPSK, BPSK, DCSK, I-CDPK (synchronization delay=1000) and ½ I-CDPK (synchronization delay=100). Our paper deals with the comparative study of these modulation techniques. I-CDPK with calculative synchronization delay gives the better response then these all. Chaos based secure communication has been of much interest in the recent time since it offers potential advantage over conventional methods due to its simplicity and high unpredictability which means higher security. Besides, analog implementation is possible.

Keywords: I-CDPK algorithm, Synchronisation delay, chaotic system, MACT, MACR, DPSK, BPSK, DCSK, I-CDPK, ½ I-CDPK

1. INTRODUCTION

In digital communication we try to getting high data rate better response lower BER and secured communication. Chaotic communication is type of secured communication.

Nowadays, with advanced synchronization schemes, chaotic systems have been widely applied to digital communications, especially in the topics of channel coding [1–2], channel modulation [3–4] and multiple accessing [5–6]. In conventional digital communication systems, channel modulation mechanism maps the digital data to analog signals so that they can be transmitted to the band-limited channel. These analog signals could be some proper pieces of chaotic signals in the digital communication systems using chaotic modulations—chaos shift keying (CSK) [3] and differential chaos shift keying (DCSK) [7], for instance. With the goal of extracting the transmitted digital data from the received chaotic signals, correlator-based receivers [8, 9] are usually adopted.

Interleaved chaotic differential peaks keying (I-CDPK) modulation technique is improve the channel efficiency. The input digital bits are interleaved by all states of the chaotic circuit and only one state is necessary to be sent to the receiver through the public channel. By means of the observer-based chaotic synchronization technique, the transmitted and interleaved digital bits can be reconstructed correctly by synchronizing the chaotic circuits of the transmitted and the receiver at arbitrary rate.

Moreover, there is no need for correlators in the proposed system, since the I-CDPK uses the difference between the current and next peak values of chaotic signal to decide bit ‘‘1’’ or ‘‘0’’. In contrast with the correlator based communication system, the total noise power at the decision instant is independent of the transmitted signal energy in the proposed non-correlator based communication system. For a practical application, the FM modulator/ demodulator and additive white Gaussian noise (AWGN) in channel are taken into account [10]. Furthermore, the performance of bit error rate of the proposed system in this paper is analyzed and compared with those of coherent BPSK and coherent DCSK.

2. DIGITAL MODULATION TECHNIQUE USED IN CHAOTIC COMMUNICATION

- **DPSK:**
  The differential phase shift keying (DPSK) is a well known technique, where the information is coded in the phase difference between two subsequent segments of a harmonic waveform [11]. These waveform segments have a given length T_b and each segment serves as the reference for the following one. If their phase difference is zero, a ‘‘1’’ symbol was transmitted. If we find a phase difference π, the transmitted symbol was ‘‘-1’’.

- **DCSK:**
  In DCSK, every symbol to be transmitted is represented by two sample functions. The first sample function serves as a reference while the second one carries the information. In the case of binary transmission, bit 1 is sent by transmitting a reference signal provided by the chaos generator twice in...
succession. For bit 0, the reference chaotic signal is transmitted, followed by an inverted copy of the same signal.[12] The two sample functions are correlated in the receiver and the decision is made by a level comparator.

\section*{BPSK:}
In the case of BPSK, two symbols are used to transmit the bit stream \( b_n \). Thus, the signal set contains two sinusoidal signals \( s_1(t) \) and \( s_2(t) \). [13] The binary symbols 0 and 1 are mapped to the signals

\[ s_1(t) = \frac{2E_b}{T} \cos(\omega_c t) \]

and

\[ s_2(t) = -\frac{2E_b}{T} \cos(\omega_c t) \]

Respectively, where \( 0 \leq t < T, T = T_b \) and \( E_b \) is the transmitted energy per bit.

\section*{I-CDPK:}
The CDPK scheme proposed in [14] only uses one state of chaotic circuit to represent the transmitted digital data. However, I-CDPK modulation scheme [10] can improve the channel efficiency by bearing the interleaved input digital bits over all states, but only one system state is necessary to be sent to the receiver through the public channel.

If \( U_{j+1} - U_j \geq \alpha > V_{th} \) or \( L_{j+1} - L_j \geq \alpha > V_{th} \), then mark as bit “1”.

If \( U_{j+1} - U_j \leq \beta < V_{th} \) or \( L_{j+1} - L_j \leq \beta < V_{th} \), then mark as bit “0”.

where \( U1, U2, U3 \) and \( U4 \) denote the successive upper peak values, while \( L1, L2 \) and \( L3 \) are the successive lower peak values of state \( x_3 \) Rössler – like chaotic circuit evolved in time; while, \( \alpha \) and \( \beta \) are noise threshold voltages to against the channel noise, and \( V_{th} \) is the decision threshold voltage. The same encoding rule can be applied to other states of chaotic circuit so that all states bear the interleaved input digital information. Where the Guard Bits are used to skip transient period occurring at the beginning of each perturbation and the Synchronization Bits are used to inform the receiver to detect the Transmitted Bits.

\section*{½ I-CDPK:}
When I-CDPK is applied at synchronization delay 100 then it is called ½ I-CDPK. It is just special case of I-CDPK. Synchronization delay is an effective parameter in communication studies. “Synchronization delay is delay between groups of bit synchronize during the transmission”. Synchronization delay will minimize in this paper to reduce the length of bit train and the reducing the bit error rate.

\section*{3. SYNCHRONIZATION TYPE}
In this paper we have used ‘S’ type chaotic flow. Cases D-S all have similar structure and topologically resemble the Rössler attractor in that they are dominated by a single folded band. There are 19 types of chaotic flows (A-S). [14]

\[ \dot{x}_1 = -x_1 - 4x_2, \quad \dot{x}_2 = x_1 + x_2^3, \quad \dot{x}_3 = 1 + x_1, \quad y = x_3 \] ............ (1)

Equ. (1) Has one positive Lyapunov exponent of 0.188 and fractal dimension of 2.151. Then the MACT’s chaotic circuit can be rewritten by the matrix form:

\[ \begin{bmatrix} x \n y \n 0 \end{bmatrix} = \begin{bmatrix} -1 & -4 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x \n y^2 \n 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \n 1 \end{bmatrix} (d), \]

\[ \equiv Ax + f(y) + Bd. \]

\[ y = x_3 = [0 \ 0 \ 1]x, \equiv c^T x. \] ............ (2)

Observer gain is \( L^T = [54.01 - 13.0075 \ 14] \)

\section*{4. ARCHITECTURE OF MULTIPLE-ACCESSING CHAOTIC DIGITAL COMMUNICATION SYSTEM}
Before introducing the proposed chaotic multiple access scheme, it is necessary to describe some current major multiple access schemes as comparisons. In FDMA, each link is assigned to a different frequency band so that all the active links can share the channel at the same time. Comparing with FDMA, TDMA allows users to create link at the same frequency band by separating every link into different time slots. A well-know application of TDMA is its utilization in the second-generation (2G) mobile phone system, i.e. GSM system. In CDMA, by specifying different codes for every link, different users can create.

In comparison with the above mentioned multiple access schemes, the key difference is that every link is assigned to a different state of the chaotic system. The transmission between all the three links can be achieved on the same frequency band at the
same time without the need of the codes used in CDMA, different frequency bands for different transmitter/receiver pairs in FDMA and the separated time slots for all the links in TDMA. In the proposed system as shown in Fig.1, there are total three Links, which are Link 1, Link 2 and Link 3. Every three serial input bits from each Link will be combined to nine parallel bits as the input bits to Chaotic Transmitter, i.e. I-CDPK Modulator (ICM) [15].

As mentioned above, every Link is assigned to a system state of the transmitter’s chaotic circuit. The detail operations of the multiple-accessing chaotic transmitter will be addressed in the following two sections. Then, the output of the multiple-accessing chaotic transmitter is fed into FM transmitter. From the public channel, FM receiver extracts the transmitted chaotic signal as the input of the multiple-accessing chaotic receiver, i.e. I-CDPK Demodulator (ICDM) [16].

Finally, the transmitted every three bits from each Link in a transmission, will be received by demodulating the corresponding recovered system state of the chaotic circuit in the I-CDPK demodulator.

1. Start the off-lined self-learning process.

2. Sample all states of the free running chaotic circuit in the I-CDPK Modulator (ICM).

3. Digitize these samples, detect local peak values of all system states, and store these values into the buffer.

4. Search for the specified $s$ synchronization bits binary code from every $g+s+1$ consecutive peak values in all the peak value buffers and then the $N/L$ input bits binary code of every individual Link form every $−1$ consecutive peak values in corresponding peak value buffer.

5. Push the first peak value of the consecutive series obtained in Step 4 and the digitized samples at this moment into the I-CDPK Modulator (ICM) parameter memory.

**Fig. 1: The proposed Multiple Access Chaotic Digital Communication system**

**I-CDPK Modulator (ICM):**

The detailed modulating procedures of the I-CDPK modulation are summarized as follows:

1. Start the off-lined self-learning process.

2. Sample all states of the free running chaotic circuit in the I-CDPK Modulator (ICM).

3. Digitize these samples, detect local peak values of all system states, and store these values into the buffer.

4. Search for the specified $s$ synchronization bits binary code from every $g+s+1$ consecutive peak values in all the peak value buffers and then the $N/L$ input bits binary code of every individual Link form every $−1$ consecutive peak values in corresponding peak value buffer.

5. Push the first peak value of the consecutive series obtained in Step 4 and the digitized samples at this moment into the I-CDPK Modulator (ICM) parameter memory.
6. Repeat from Steps 2 and 5 until all the parameters matching every $N$ bits binary codes have been found.

7. Stop the off-lined self-learning process and start the transmitting period.

8. Combine all $N/L$ input bits from each Link into $N$ input bits set, then the Parameters Output mechanism will read the stored parameters corresponding to this $N$ bits set from the parameters memory and send them to perturb the signals of the chaotic circuit through the D/A converter.

9. Repeat Step 8, until the transmitting period is stopped.

5. BIT ERROR RATE ANALYSIS

The $I$-CDPK uses the difference between the current and next peak values of chaotic signal to decide bit “1” or “0”. During the transmitting, the channel noise will cause that these received peak values deviate from those of the transmitted signal. Once the received differential peaks cross the threshold $V_{th}$ at the decision instant, the bit-errors occur. In this section, an error analysis model will be derived to estimate BER (bit error rate) of the proposed system.

In order to compare the BER performance between $\frac{1}{2}$ I-CDPK, I-CDPK, BPSK, DPSK and DCSK, the BER of coherent BPSK, coherent DPSK and that of coherent DCSK are given by

$$\text{BER}_{\text{BPSK}} = \frac{1}{2} \text{erfc} \left(\frac{E_b}{N_0}\right)^{1/2}$$

$$\text{BER}_{\text{DCSK}} = \frac{1}{2} \text{erfc} \left(\frac{E_b}{2N_0}\right)^{1/2}$$

$$\text{BER}_{\text{DPSK}} = \frac{1}{2} \exp \left(-\frac{E_b}{N_0}\right)$$

where erfc($z$) is the complementary error function and $E_b$ denotes the symbol energy per bit.

Hence, the estimated BER of I-CDPK and $\frac{1}{2}$ I-CDPK can be modified as follows:
BER = \frac{1}{2} \text{erfc} \left( \frac{2E_b}{N_0} \right)^{1/2} \\
\approx \frac{1}{2} \text{erfc} \left( \frac{Z}{\sqrt{2}} \right)

(\text{Since } Q(z) = \frac{1}{2} \text{erfc} \left( \frac{Z}{\sqrt{2}} \right))

\text{BER} = \frac{1}{2} \text{erfc} \left( \frac{2E_b}{N_0} \right)^{1/2}

(\text{Since } Q(z) = \frac{1}{2} \text{erfc} \left( \frac{Z}{\sqrt{2}} \right))

6. RESULT

On the basis of bit error rate response I have BER VS SNR graph given below which states that \( \frac{1}{2} \) I-CDPK gives better response as compared to other modulation schemes.

From the above graphs and table it is clear that \( \frac{1}{2} \) I-CDPK or I-CDPK at synchronization delay 100 gives better BER response as compared to other modulation schemes with different parameters.

\( \frac{1}{2} \) I-CDPK gives the bit error rate reduction as compared to other schemes.

Table.1 Reduction in BER w.r.t \( \frac{1}{2} \) I-CDPK

<table>
<thead>
<tr>
<th>SNo.</th>
<th>Modulation Schemes</th>
<th>Reduction in BER w.r.t ( \frac{1}{2} ) I-CDPK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I-CDPK</td>
<td>( \approx 50% )</td>
</tr>
<tr>
<td>2</td>
<td>BPSK</td>
<td>( \approx 92% )</td>
</tr>
<tr>
<td>3</td>
<td>DCSK</td>
<td>( \approx 96% )</td>
</tr>
<tr>
<td>4</td>
<td>DPSK</td>
<td>( \approx 97% )</td>
</tr>
</tbody>
</table>

7. CONCLUSION

I have taken different modulation schemes such as BPSK, DCSK, DPSK and I-CDPK and observed that their response at different synchronization delay. I have seen that BER response at synchronization delay 100 gives about \( \approx 50\% \) reduction in BER at synchronization delay 1000 for all modulation schemes and \( \frac{1}{2} \) I-CDPK gives BER reduction about \( \approx 50\%, \approx 92\%, \approx 96\% \) and \( \approx 97\% \) for I-CDPK, BPSK, DCSK and DPSK.

REFERENCES


