Analysis of Traff’s Current Comparator in 90 nm CMOS Technology

Adyasha Rath¹, Subhrajyoti Das², Sweta Padma Dash³, Geeta Pattnaik⁴, Adyasa Samantaray⁵
¹, ², ³, ⁴, ⁵ M.Tech Student, School of Electronics Engineering, KIIT University, Bhubaneswar, India

ABSTRACT
In this paper the Traff’s current comparator is designed using a current differencing stage is seen which compares an input current with a reference current maintaining high speed and low power. Earlier works of current comparator neglected the current differencing stage although the current differencing stage forms an important part of the current comparison process. The circuit has been simulated in Cadence EDA tool in 90nm CMOS process technology using Spectre simulator. Transient response confirms the very high speed operation of the Current Comparator when the current differencing stage is added.

Keywords – current difference, delay, positive feedback, reference current, Traff’s current comparator

I. INTRODUCTION
Comparators have always formed a vital component for a varied type of analog systems including data convertors and other front-end signal processing applications. Many sensors such as temperature sensors and photo sensors produce current signal as output which can be compared using a current comparator. The reduction in device sizes has motivated the analog designers to design devices using the current mode approach. Apparently the current-mode approach is found to be advantageous in terms of speed, bandwidth, and decreased the need of high supply voltages. However, high performance current mode comparators have not been frequently published, and only a few structures exist.

A very crucial component of this ADC is a current comparator. It is a fundamental building block of current-mode ADCs in order to increase the conversion speeds. To a great extent this conversion speed depends on the current comparator. However, in current comparator design, trade-off between speed and power dissipation occurs. A low power design would mean lower speed and vice versa. The current comparison process involves injecting one or two currents into the comparator and distinguishing if the current (or the difference of two currents) is positive or negative. Other requirements include low input impedance and rail-to-rail output voltage swing.

The first CMOS current comparator was proposed by D. Freitas and K. Current in [1]. Since then, many high performance current comparators have been proposed. H. Traff presented a simple and high-speed current comparator in [2], but the output swing of Traff’s comparator could not reach the power supply rails. Some generalised implementations of the Traff’s comparator have been carried out in [3] – [10].

In this work the Traff’s Current comparator [2] shows improved performance when a current difference stage is added. Previously current comparators neglected the current differencing circuit which takes two currents as input, one as reference current with respect to which the input current input current is compared. Simulations were carried out in 90nm process technology in Cadence using EDA tool.

II. BASIC CURRENT COMPARATOR CONCEPTS
A current comparator determines if a current signal exceeds a given threshold and produces an output voltage. A current-mode comparator receives an input signal in the form of a current and compares it to a pre-defined threshold current. The output is in the form of a voltage.

An ideal current comparator would allow the input signal to settle very quickly, i.e. there would be no capacitance on the input and it would be able to take an infinitely small change in current and convert it into voltage at the output of the device. Fig 1 shows the transfer characteristics of an ideal current comparator. \( V_{OL} \) and \( V_{OH} \) in the figure denote the limiting values of the output logical states.

![Fig. 1 Current Comparator Characteristics](image)
A current comparator basically consists of three different stages:
(1) Current Difference Stage
(2) Gain Stage
(3) Output Stage

The current comparator works as follows:
When the reference current (Iref) is greater than the input current (Iin) the comparator output is logic low and vice-versa.

\[
\begin{align*}
I_{\text{in}} &> I_{\text{ref}}, \quad V\text{out} = 1 \\
I_{\text{in}} &< I_{\text{ref}}, \quad V\text{out} = 0
\end{align*}
\]

### III. TRAFF's CURRENT COMPARATOR WITH CURRENT DIFFERENCING STAGE

The current comparator takes current as input and produces voltage as output. When the input current Iin is greater than the reference current Iref, the output voltage is logic high i.e. is pulled to V_{DD}. Similarly when the input current is less than the reference current the output voltage is logic low. In Fig. 2 the current differencing stage is shown which consists of transistor M1-M12. The current differencing stage takes two input currents. Generally for convenience we take one as input current (Iin) and another as reference current (Iref). The reference current is the threshold current with which the input current is to be compared.

The Traff’s comparator as shown in Fig. 3 consists of transistors MN-MP which pair up to form a class B voltage buffer. The transistors M13-M18 form a cascade of three CMOS inverters. The inverter M13-M14 provides a positive feedback at node 1 thus lowering the input impedance help in producing a rail-to-rail output voltage.

### IV. SIMULATION & RESULTS

The current comparator was simulated in 90nm process technology in Cadence using Spectre simulator in Virtuoso platform. The reference current Iref was taken as 1µA and the input current Iin was varied from 0.5µA to 1.5µA. The input current is generally taken as I_{\text{in}} = I_{\text{ref}} \pm \Delta I. \Delta I refers to the difference of input current from the reference current. In our case the difference current was taken to be, \( \Delta I = \pm 0.5 \) µA. With V_{DD} = 0.9V the transient analysis of the circuit was carried out as shown in figure. The transient response shown in Fig. 4 indicates the speed of the current comparator.

The delay was found to be 0.72ns. Hence the speed of operation was found to be 1.4GHz. The average power consumption of the comparator was found to be 116.4µW. The PDP of the current comparator was found to be 0.084pJ.
The corner analysis of the above current comparator was carried out. It was seen to perform in all corners i.e TT, FS, SF and SS except the FF corner. The corner analysis results are seen in Table I.

<table>
<thead>
<tr>
<th>Corner</th>
<th>Delay (ns)</th>
<th>Power (µW)</th>
<th>Slew Rate (V/ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>0.72</td>
<td>116.4</td>
<td>4.399</td>
</tr>
<tr>
<td>FS</td>
<td>0.79</td>
<td>124.9</td>
<td>3.211</td>
</tr>
<tr>
<td>SF</td>
<td>0.69</td>
<td>88.12</td>
<td>6.646</td>
</tr>
<tr>
<td>SS</td>
<td>0.82</td>
<td>59.93</td>
<td>7.675</td>
</tr>
</tbody>
</table>

In Fig. 5 and Fig. 6 the variation of delay and power with the current difference is plotted.

Fig. 5 Variation of Delay with Current Difference

The plot of PDP (Power Delay Product) against current difference is shown in Fig. 6. It is seen that the PDP decreases as current difference between the reference and input current increases.

Fig. 6 Variation of Power with Current Difference

Fig. 7 Variation of PDP with Current Difference

The layout of the Traff comparator design is done using Layout XL tool available in Cadence as shown in Fig. 8.

Fig. 8 Layout of Traff’s Comparator in 90 nm CMOS process technology

V. CONCLUSION

The Traff’s current comparator was found to exhibit a speed of 1.4GHz at a current difference of ±0.5 µA. The average power consumption of the comparator was found to be 116.4µW thus making it suitable for low power applications.

REFERENCES


