SURVEY ON USB 3.0-ARCHITECTURE, DATA TRANSFER TECHNIQUE, POWER MANAGEMENT AND OPTIMIZATION OF CURRENT LIMITING SOLUTIONS

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Abstract: As 21st century is known as the era of technology and electronics. Within a few decades, there is high growth in the field of electronics, so regarding to connections between computers and electronics devices, USB (Universal Serial Bus) is used. USB is the dominant interface for external computer peripherals. It is standard for wired connection between two electronic devices (with maximum speed of 5Gbps), including a mobile phone and desktop computer. USB 3.0 utilizes dual bus architecture which provides both Super Speed and non-Super Speed connectivity. The need for Super Speed data communication leads to the use of USB 3.0. In this paper we discuss the Architecture of USB 3.0, Data Transfer Technique, Power Management and Optimization of Current limiting solutions.

Keywords – Universal Serial Bus, Super Speed USB, PPTC

1. Introduction
The Universal Serial Bus is a standard communication interface developed for interconnection between computer and peripheral devices. The peripherals include pointing devices, keyboard, printers, digital cameras, etc. The bus supports the plug and play feature. This implies that there is no need to open up the PC while adding a new device and allowing the software to get installed automatically. It provides low cost, bi-directional and high speed data transfer.

The USB has the following key features:

1. Single Connector Type: USB replaces all the different legacy connectors with one well-defined, standardized USB connector for all USB peripheral devices, eliminating the need for different cables and connectors and thus simplifying the design of the USB devices. So all USB devices can be connected directly to a standard USB port on a computer.

2. Hot-swappable: USB devices can needed while the computer is running. So there is no need to reboot.

3. Plug and Play: Operating system software automatically identifies, configures, and loads the appropriate device driver when a user connects a USB device.

4. High performance: USB offers low speed (1.5 Mbit/s), full speed (12 Mbit/s) and high speed (up to 480 Mbit/s) transfer rates that can support a variety of USB peripherals. USB 3.0 (Super Speed USB) achieves the throughput up to 5.0 Gbit/s.

5. Expandability: Up to 127 different peripheral devices may theoretically be connected to a single bus at one time.

6. Power supplied from the bus: USB distributes the power to all connected devices eliminating the need for external power source for low-power devices. High-power devices can still require their own local power supply. USB also supports power saving suspend/resume modes.

7. Easy to use for end user: A single standard connector type for all USB devices simplifies the end user's task at figuring out which plugs go into which sockets. The operating system automatically recognizes the USB device attachment and loads appropriate device drivers.

8. Low-cost implementation: Most of the complexity of the USB protocol is handled by the host, which along with low-cost connection for peripherals makes the design simple and low cost. [1]
2. History of USB:

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3.1. INTRODUCTION TO USB 3.0
The Universal Serial Bus 3.0 Specification Revision 1.0 was released in November 2008, with the first USB 3.0 device-controller hardware expected to follow about a year later.
USB 3.0 defines new dual-bus architecture (Fig-1) with two physical buses that operate in parallel. USB 3.0 provides a pair of wires for USB 2.0 traffic and additional wires to support the new Superspeed bus at 5 Gbps. Super Speed offers a more than 10 time increase of data transfer than over USB 2.0 high speed. [2]

3.2. USB 3.0 Superspeed Architecture
Superspeed architecture consists of the following elements.

**Superspeed Interconnect:** It is the manner on which devices are connected and communicate with the host over the Superspeed bus. This includes topology, communication layer and how they interacted to accomplish the data exchange.

**Devices:** Devices are sources or sinks of information exchanges. They implemented the required device end, Superspeed communication layers to accomplish data exchange between drive on the host and logical functions of the devices.

**Host:** It holds the Superspeed data activity schedule and management of the Superspeed bus and all the devices connected to it. [3]

3.3. USB 3.0 Communications Layers and Power Management Elements

3.3.1. Physical layer
- The physical layer defines the PHY portion of a port and physical connection between a downstream facing port and upstream facing port of the device.
- Superspeed physical connection is the comprised of two differential data pairs transmit and receive path. The nominal data rate is 5Gbps.

Fig-1 USB 3.0 Bus Communication
Fig-2 USB 3.0 Superspeed Architecture
3.3.2. Link Layer
It is logical and physical connection of the two ports. **Logical portion include**
- Initialization of physical layer and event management i.e. connect removal and power management.
- State machines and buffering for managing information exchanges. It implements protocol for flow control, reliable delivery of packet headers, and link power management.
- Buffering for data and protocol layer information elements.
- Detect receive packets and error checks for received header packets.
- Provide an appropriate interface to the protocol layer for information exchanges.

3.3.3. Protocol Layer
- It defines end to end communication rules between a host and device.
- Protocol communications are accomplished via the exchange of packets. These packets are sequence of data with specific control sequence.
- Packet headers are the building block of protocol layer.[5]

4.1. Data transfer Technique
Data and control exchanges between the host and devices are via sets of either unidirectional or bi-directional pipes.
- Data transfers occur between host software and particular endpoint on a device.
- Most pipes come into existence when device is configured by system software.
- The pipes support one on or more transfer types.
- Bulk transfer has extension for Superspeed called stream which is in-band protocol-level support for multiplexing multiple independent logical data stream through a standard bulk pipe.[6]

4.2. Superspeed Data Flow Model
Superspeed is very similar to USB2.0 in which it provides communication service between a USB host and attached USB devices. The concept behind Superspeed data flow is:
- **Communication flow models:** flows between the host and devices through the Superspeed bus
- **Superspeed protocol overview:** It gives a high level overview of the Superspeed protocol.
- **Transfer Description:** It provides an overview of how data transfers work in Superspeed and subsequent sections defines the operating constraints for each transfer type.
- **Device Notifications:** It a feature which allows a device to asynchronously notifies its host of events or status on the devices.
- **Reliability and Efficiency:** It summarized the information and mechanisms available in Superspeed to ensure reliability and increase efficiency.

5. Power Management of USB 3.0
The SuperSpeed architecture has been defined with platform power efficiency as a primary objective.
Some of the power efficiency enhancements is:
- Elimination of continuous device polling.
- Elimination of broadcast packet transmission through hubs.
- Introduction of link power management states enabling aggressive power savings when idle.
- Device and individual Function level suspend capabilities
- enabling devices to remove power from all. Host and device initiated transition to low power states [6].
6.1. Optimization of USB 3.0 Current Limiting Solution
In addition to transfer speed enhancement in USB 3.0, the requirement for power supply is also increased to meet various peripheral demands. Hence Polymeric Positive Temperature Coefficient (PPTC), which is an over-current protection device often used in the industry. With the use of USB 3.0 the transfer speed increase to a blazing 5.0 Gbps, the power budget was also boosted from 500mA to 900mA. The increase in speed and power brings new challenges to both system and component level, from integrating new data transfer protocol and new power management schemes, to successfully transferring data between host and device.

6.2. PPTC Introduction and Over-Current Protection.
Polymeric Positive Temperature Coefficient, commonly known as PPTC, can be treated as a non-linear temperature-dependant resistor. Under normal operation, PPTC is highly conductive so the circuit can operate normally. However, if an over-current event occurs, faulty current will generate enough heat on PPTC to exceed its switching temperature, causing a 10^4 to 10^6 times resistance jump. Therefore, the over-current condition can be eliminated, and the objective of protecting the circuit device can be achieved. Due to the increase of power budget in USB 3.0, current limiting devices must pass through more power and keep a voltage drop limit. Fig-4 shows PPTC having more advantages than low-voltage solid-state switches in USB 3.0 application, such as price, resistance, maximum fault power, and ESD sensitivity.

6.3. Power Delivery Difference from USB 2.0
Compared to USB 2.0, USB 3.0 creates new power management schemes to achieve overall platform power efficiency, by defining new link states and mechanisms. However, in terms of power distribution, USB 3.0 remains similar to 2.0, with increased power budget and more generous voltage drop requirement. SuperSpeed devices can now draw up to 900mA after initiation with the host. The supplied voltage requirement at the connector of hub or root ports has been decreased from 4.75V to 4.45V, and bus-powered devices should be capable of operating with input voltage as low as 4.00V. Other requirements such as inrush current limiting and suspend current limitation stay as stringent as before, with updated power allocation of 150mA or 900mA for high-power device.

7. Conclusion and Future Work
Through this paper, we understand the concept of USB and difference in transfer speed of USB specification. We also understand the Architecture, Communication Layer, Data Transfer technique and PPTC over current protection of USB 3.0. In future, we can understand the data bursting capability of USB 3.0 and furthermore USB 3.1 specification has been released and now the computer industry will adopt the standard and more forward to the more advanced protocol.

References

Fig 4- Comparison of PPTC and Solid-State Switch