Design and Implementation of Low Power and High Performance 0.13µm CMOS Dynamic Comparator for Analog to Digital Converter

Akanksha¹, Jaya Nidhi Vashishtha²
¹(Department of Electronics and Communication, IMS Engineering college, Ghaziabad
²(Department of Electronics and Communication, IMS Engineering college, Ghaziabad

ABSTRACT
The proposed design is a CMOS dynamic comparator using dual input double output differential amplifier as latch stage suitable for high speed analog-to-digital converters with low power dissipation and high performance. The design’s output shows lower power dissipation and higher speed than the other latch type voltage sense comparator. The proposed dynamic comparator topology is based on positive feedback where two cross coupled differential pair and two switchable current sources are used. The circuit is designed using 0.13 µm CMOS technology and the desired output obtained with 20 MHz clock frequency and 3.3V power supply.

Keywords – ADC, differential amplifier, dynamic comparator, high speed, low power

I. INTRODUCTION

High speed devices like high speed analog to digital converters, operational amplifiers became of great importance. And for high performance applications, a major attention is given towards low power dissipation. Power dissipation minimization can be achieved by moving towards smaller feature size processes. However, as we give importance to smaller circuit area, the other parameter variations and other non-idealities will greatly affect the overall performance of the device [1]. Now analog-to-digital converter requires lower power dissipation, better slew rate, high speed, less Offset.

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison. Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as analog-to-digital converter for 1 bit and for that reason they are mostly used in large abundance in analog-to-digital converter.

In the analog-to-digital conversion process, it is initial step to first sample the input. And the sampled signal is then given as input to a combination of comparators to determine the digital equivalent of the analog signal. The analog to digital signal converting speed of comparator is limited by the decision making response time of the comparator [3]. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. Apart from that, comparators are also found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, data transmission, and others.

II. DYNAMIC COMPARATOR

Dynamic comparator are the comparators which are clocked and only provide an output after the transition of the clock. The speed of clocked comparators can be very high and the power dissipation of clocked comparator can be very low. Regenerative feedback is often used in dynamic comparators and they are used in designing of high speed ADCs.

Latch type sense amplifiers are used to read the contents of the different kinds of memory, analog to digital converters, data receivers and on-chip transistors since they yield fast decision due to positive feedback [4]. These are very effective comparators. Latch type voltage sense amplifier that uses back to back latch stage to generate positive feedback.

Using this sense amplifier (SA) in low-voltage deep-sub-micron CMOS technologies is difficult because stack of the four transistors requires large voltage headroom. And also offset voltage and speed of this sense amplifier is very much dependent on the common mode voltage of the input because of which it is problematic to use this
sense amplifier in Analog-to-digital converters where wide common mode ranges are used [9].

Fig. 1. Latch type voltage sense comparator

The proposed comparator provides better input offset characteristic and faster operation. The back-to-back latch stage is replaced with back-to-back dual input single output differential amplifier stage. Differential amplifier has so many merits over the conventional latch which is nothing but an inverter. Proposed dynamic comparator rejects common mode noise or in other words it has better common mode rejection ratio. Another property of proposed dynamic comparator is the increase in maximum achievable voltage swings due to the differential scaling. It also provides simpler biasing and higher linearity. Here our main purpose is to reducing the rising and falling propagation delay of the output waveform with change in input and clock signal.

The static and dynamic characteristics of comparators are gain, output high, low states, input resolution, offset, noise and propagation delay. For ADC application, the important characteristics of dynamic comparator are gain and propagation delay [10].

Gain of the comparator can be written as:

\[
\text{Gain, } A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V}
\]  

(1)

Where \(\Delta V\) is input voltage change

Propagation delay can be defined as at how much speed the amplifier responds with applied input. Propagation delay \(t_e\) is the average of rising propagation delay \(t_r\) and falling propagation delay \(t_d\).

\[
t_e = \frac{t_r + t_d}{2}
\]  

(2)

Fig. 2. Proposed design of dynamic comparator

III. RESULT AND DISCUSSION

The output voltage is changing from logic ‘0’ to logic ‘1’, when the input voltage is larger than the reference voltage.

Fig. 3. Simulated waveform of dynamic comparator
The simulated waveform, which is produced by the proposed dynamic comparator is shown in Fig. 3. If the input is greater than the reference voltage, the output changes from the low logic to high logic at the rising edge of the clock. The output voltage does not change till the input voltage is become less than the reference voltage at the rising edge of the clock occurs.

The power dissipation of the proposed dynamic comparator is 2.141 µW and the propagation delay of the circuit is 0.1 ns with 20 MHz clock frequency.

IV. CONCLUSION

A new dynamic comparator using positive feedback which shows higher speed, low power dissipation than the latch type voltage sense dynamic latched comparators has been proposed & targeted for ADC application. The results are simulated using 0.13µm CMOS technology. In the proposed dynamic comparator design, the back-to-back inverter circuit is replaced with dual input double output differential amplifier in the latched stage. The noise present in the input and the clock is suppressed by the differential amplifiers present in the output latch stage. High speed dynamic comparators are mostly used in analog to digital comparators but they are also used in zero-crossing detectors, peak detectors, data transmission etc.

REFERENCES