Implementation of High Speed 0.13 µm CMOS Dynamic Latch Comparator

Akanksha¹, Jaya Nidhi Vashishtha²
¹Department of Electronics and communication, IMS Engineering College, Ghaziabad
²Department of Electronics and Communication, IMS Engineering College, Ghaziabad

ABSTRACT
For high speed applications, the important factors are speed, power and resolution. The CMOS dynamic comparator using dual input single output differential amplifier stage at both input and output stage is presented as a proposed dynamic comparator. The desired output of CMOS dynamic comparator circuit is obtained with 3.3V power supply voltage and 20 MHz clock frequency using 0.13 µm technology. The comparison results of various comparators indicates that the proposed comparator achieve improved switching speed and power consumption than the two state dynamic comparator. The circuit is suitable for high speed analog to digital converter, window detector, level shifter and relaxation oscillator.

Keywords - CMOS dynamic comparator, full voltage swing, high performance, power consumption, window detector

I. INTRODUCTION
Comparators plays important role in window detector, relaxation oscillator, level shifter, analog to digital converter and peak detectors etc. Basically, comparator is an electronic circuit which compares an analog signal (voltage or current) with another analog signal and gives a digital output based on the comparison of two signals [1]. As the number of transistor increases on the chip, managing the increasing power consumption is important due to heating of the chip. The factors which consider in selecting the comparators are power consumption, propagation delay, slew rate and resolution. The power consumption is crucial factor to the VLSI designers because of the growth of portable devices in the market.

The comparators which have two analog input and one clock signal input is called dynamic comparator. Mostly in dynamic comparator, positive feedback is used i.e. back to back cross coupled inverters is used for converting voltage difference to a digital signal level. The speed of clocked comparators can be very high and the power consumption of clocked comparators can be very low [2].

II. METHODOLOGY
Positive feedback is introduced by arranging two back to back latch stages. Due to which it used in different kinds of memory applications. Double tail latch type voltage dynamic comparator uses one tail for input stage and another for latching stage [10]. Fig 1 shows the schematic of double tail latch type dynamic comparator.

![Fig.1. Double tail latch type dynamic comparator (comparator 1)](image)

Fig 2 shows the schematic of two stage dynamic comparator. Except than the output latch the circuit is same. By modifying the latch, the need of two clocks is eliminated. Power consumption of the circuit is reduced.
but the propagation delay is increased due to the weak clock signal at the output stage.

**Fig.2. Two stage dynamic comparator (comparator 2)**

Now, propagation delay is reduced by introducing an inverter between input and output. Due to the inverter, weak signal produced by the input stage is regenerated and gives as the input to the output stage. Therefore, propagation delay and the power dissipation is reduced than the two state dynamic comparator.

The important characteristics which consider for comparators are speed, propagation delay, resolution and power. Propagation delay is the delay in changing the output with respect to the input. It means delay between input and output. Speed is the reciprocal of the propagation delay. Resolution is the input voltage change to make output change to valid digital state [10].

**Fig 3 shows the schematic of the dynamic latched comparator. During Reset phase, M9 and M10 PMOS transistors turns on and regenerative node charges. Due to the high input at the regenerative node NMOS transistors M11 and M16 turns on. Therefore, output of the inverter discharges to ground and make output nodes charged to VDD and then M13 and M15 turns off due to the high drain voltages compare to gate voltage.**

**Fig.3. Proposed dynamic latched comparator (Comparator 3)**

**III. RESULTS AND DISCUSSION**

The simulated output waveform which is produced by the proposed dynamic latched comparator is shown in fig 4. At the reset phase, the output is high and when the clock is high, the output is changed according to the difference between the input and reference signal i.e. if the input signal is greater than the reference signal then the output is at high logic and vice versa.
The power dissipation and propagation delay of the proposed dynamic latched comparator is 0.192 µW and 0.22 ns. It is very less as compare to the power dissipation 20.80 µW and propagation delay 14.78 ns of the two stage dynamic comparator. All the values are calculated at 20 MHz clock frequency with 3.3 V of power supply.

IV. CONCLUSION

The proposed dynamic latched comparator provides high switching speed and less power consumption as compare to the two stage dynamic comparator at specific clock frequency. This type of comparator is suitable for analog to digital comparator, window detector and level shifter etc. The results are simulated using 0.13 µm CMOS technology.

REFERENCES