A New Approach Ultra Low Voltage CMOS Logic Circuits Analysis

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ABSTRACT
The operation of digital circuits from power supply voltage of the order of 200mv or less imposes that, in general MOSFETs biased in the sub threshold regime, characterized by the exponential relation between the control voltages and the current. In this paper we analyze some of the basic building blocks of digital circuits operating in the sub threshold region. We analyze the basic CMOS inverter as regards the voltage transfer characteristics, dynamic behavior, and power dissipation. To reduce the dependence of the drain current on the process parameters we show some compensation circuits that adjust the body voltage, with a small silicon area penalty.

Keywords - Ultra low voltage logic, sub threshold, low power.

I. INTRODUCTION
In recent years, significant advances toward ultra-low voltage have been achieved, aimed at applications that are energy autonomous or rely solely on small batteries. Examples of these applications include cell phones, laptops, handheld and wearable computing, and biomedical systems [1], [2]. All of these applications must save energy while providing intelligence and better performance for costly infrastructure and support in places with difficult access, such as inside the human body. Moreover, in the future most electronic devices will include a wireless connection, leading to millions of connected devices [3]. All of these devices must capture their own energy, since it is not feasible to use batteries in all of them; nature would simply be unable to absorb all of these batteries after their disposal. In this regard, a reduction in the supply voltage is the most important action required to increase autonomy. The fundamental limit of the supply voltage in CMOS digital circuits is 36mV at 300K, as determined in [4], [5]. One of the challenges associated with lowering the supply voltage of digital circuits is to compensate for the variation in the technological parameters, mainly the threshold voltage, V_T, of the transistors. Threshold voltage spreading from wafer to wafer in a given technology can lead to large variations in the drain current [6]. As a result, the performance of a digital gate can be severely degraded.

Body biasing has been applied to digital circuits in an attempt to approach the limit of supply voltage and also, to some extent, to compensate for the spreading of process parameters from wafer to wafer. It has been demonstrated that digital circuits can operate from supply voltages of 100 mV, 50 mV, and 85 mV in [6], [7], and [8], respectively.

II. CMOS INVERTER
For widely using of CMOS technology is basically for consuming less power. But as the technology feature size shrink sub- threshold leakage current is increases as the decrease of threshold voltage. In this design criterion it focuses on sub threshold leakage power consumption and it also focuses on body biasing effect and stack effect. Finally we explain the switching power and delay trade-off of generic CMOS circuit.

2.1. Static Analysis
As the supply voltage is reduced to values lower than the threshold voltage, V_T, of the NMOS and PMOS transistors, the transistors are biased in the sub threshold or weak inversion regime of operation. This regime is characterized by the exponential dependence of the drain current on the gate, drain and source voltages [10], given by (1)

$$I_{DN(P)} = I_{ON(P)} e^{\frac{V_{GB(SC)} - V_{TN(P)} - n_{N(P)} \phi_t}{n_{N(P)} V_{SB(BS)}}} \left( 1 - e^{\frac{V_{DS(SD)}}{\phi_t}} \right)$$ (1)

I_{ON(P)} is a current scaling factor which is dependent on the technology and the geometric parameters. V_{GB} and V_{SB} are the gate and source voltages referenced to the bulk and V_{DS} is the drain-source voltage. $\phi_t$ is the thermal voltage and $n$ is the slope factor. The strength or current capability of the transistor is given by.

$$I_{N(P)} = I_{ON(P)} e^{\frac{V_{TN(P)}}{n_{N(P)} \phi_t}}$$ (2)
Fig. 1: Static CMOS inverter.

Considering the standard CMOS inverter in Fig. 1, the voltage transfer characteristic (VTC) can be determined from (1). For the sake of simplicity let \( n_N = n_P = n \). The static transfer function of the inverter is obtained from

\[
I_{DN} = I_{DP} \left( e^{\frac{V_{DD}-V_{IN}}{n\varphi_t}} \right) \frac{V_{DD}}{n\varphi_t} + \left( 1 - e^{\frac{V_{DD}-V_O}{\varphi_t}} \right) = I_{OP} \left( e^{\frac{V_{DD}-V_{IN}}{n\varphi_t}} \right) \frac{V_{DD}}{n\varphi_t} + \left( 1 - e^{\frac{V_{DD}-V_O}{\varphi_t}} \right) \frac{V_{DD}}{2} \ln \left( \frac{I_{OP}}{I_{ON}} \right) \tag{3}
\]

\[
I_{ON} \cdot \frac{n\varphi_t}{2} \ln \left( \frac{V_{DD}-V_O}{n\varphi_t} \right) = I_{OP} \cdot \frac{n\varphi_t}{2} \ln \left( \frac{I_{OP}}{I_{ON}} \right) \tag{4}
\]

\[
V_I = \frac{V_{DD}}{2} + \frac{V_{TN}-|V_{TP}|}{2} + \frac{n\varphi_t}{2} \ln \left( \frac{I_{OP}}{I_{ON}} \right) + \frac{n\varphi_t}{2} \ln \left( \frac{V_{DD}-V_O}{V_O} \right) \tag{5}
\]

The VTC characterized by equation (5) is dependent on the supply voltage, the imbalance of the transistor threshold voltages and the ratio between the scaling currents. In the ideal case of transistors with the same strength, i.e., \( I_{ON} = I_{OP} \) and \( V_{TN} = |V_{TP}| \), the VTC reduces to that given by equation (6).

\[
V_I = \frac{V_{DD}}{2} + \frac{n\varphi_t}{2} \ln \left( 1 - e^{\frac{V_{DD}-V_O}{\varphi_t}} \right) \tag{6}
\]

The inverter threshold voltage, \( V_M \), is defined as the voltage, such that \( V_I = V_O \). A first order approximation of \( V_M \) derived from (5), given in (7), shows linear dependence of \( V_M \) on the threshold voltage mismatch and a logarithmic dependence on the transistors current ratio.

\[
V_M = \frac{V_{DD}}{2} + \frac{V_{TN}-|V_{TP}|}{2} + \frac{n\varphi_t}{2} \ln \left( \frac{I_{OP}}{I_{ON}} \right) \tag{7}
\]

\[
\frac{dV_O}{dV_I} \bigg|_{V_O = V_{DD}} = \frac{V_{DD}}{n} \tag{8}
\]

The dependence of \( V_M \) on the technological parameters is attenuated by the denominator in (7) which has a term that is dependent on the supply voltage according to expression (8).

For \( n = 1 \), the denominator in (8) is only 1.02 for \( V_{DD} = 200 \text{ mV} \), but it is 1.62 for \( V_{DD} = 50 \text{ mV} \). Thus, as the supply voltage is reduced the influence of the process parameters on \( V_M \) is also reduced. For \( V_{DD} > 4\varphi_t \), \( VM \) can be rewritten as

\[
V_M = \frac{V_{DD}}{2} + \frac{V_{TN}-|V_{TP}|}{2} + \frac{n\varphi_t}{2} \ln \left( \frac{I_{OP}}{I_{ON}} \right) \tag{9}
\]

The current through the inverter, \( I_{SC} \), can be calculated from (1) and (5) for any input voltage, giving (10) as a result. In particular, the maximum current, \( I_{SC \text{ MAX}} \), is given in (11) when the input voltage is equal to the logic gate threshold voltage, i.e., \( V_I = V_M \).

\[
I_{SC} = \sqrt{I_{ON} \cdot I_{OP}} \sqrt{\left( 1 - e^{\frac{V_O}{\varphi_t}} \right) \cdot \left( 1 - e^{\frac{V_{DD}-V_O}{\varphi_t}} \right)} \tag{10}
\]

\[
I_{SC \text{ MAX}} = \sqrt{I_{ON} \cdot I_{OP} e^{\frac{V_{DD}-V_{TN}-|V_{TP}|}{2n\varphi_t}}} \tag{11}
\]

Figure 2.1.1. shows the VTC and the drain current of the inverter for different supply voltages, \( I_{ON} = I_{OP} = 1 \text{nA}, n = 1 \) and \( V_{TN} = |V_{TP}| = 0.3 \text{V} \). It can be noted that as the supply voltage is reduced, the output of the inverter does not fully reach the supply rails. As an example, for \( V_{DD} = 50 \text{ mV} \), the output is 46.6 mV when the input is 0V and it is 3.4 mV when the input is 50 mV. Practical values can be even lower since the slope factor of the transistors, \( n \), is generally greater than unity.

III. PREVIOUS APPROACHES

3.1. THE NAND GATE

The analysis carried out for the inverter input-output relation, which resulted in (5) and (7), can be extended to more complex logic gates such as the NAND gate, which is shown in Fig.3.1. The output changes state for one of the two following events. In the first case, labelled as (a)
in (23), one of the inputs, e.g., $V_A$, changes whereas the other is held constant at (or close to) $V_{DD}$. In the second case, labeled as (b) in (23), both inputs vary simultaneously, i.e., $V_A = V_B$. In this case, the NAND gate is equivalent to an inverter with a P-channel transistor equivalent to the parallel association of P1 and P2 and an NMOS transistor equivalent to the series association of N1 and N2. The equivalent strength, $I_{EQ}$, of the series/parallel associations of the NAND transistors is given in (23).

$$I_{EQ-P} = I_P \quad I_{EQ-N} = I_N \quad 23(a)$$
$$I_{EQ-P} = I_P \quad I_{EQ-N} = \frac{I_N}{2} \quad 23(b)$$

The relations in (23) reveal that the threshold $V_M$ of the logic gate is dependent on whether one input varies alone or both vary together. Figure 7 shows the VTC of the NAND gate obtained from equation (5) with conditions (a) and (b) in (23) for $V_{DD} = 150\text{mV}$.

The series/parallel association of transistors can be extended to logic gates with more inputs without any degradation in the output voltage due to the transistor stacking.

3.2. BODY BIAS COMPENSATION:

The transistor drain current in the sub threshold region, equation (1), is very sensitive to $V_T$. Typical variations of $V_T$ from batch to batch can lead to considerable current variation. Figure 3.2. shows the simulation of the typical current $I_{DN(P)}$ transfers versus the gate-to-source voltage with nominal threshold voltages close to 500mV and ±30mV variations, for a 180nm technology. The current can vary by as much as a factor of five in the exponential region.

Variations in the process parameters result in shifts in the voltage transfer characteristic (VTC) of a CMOS inverter, as can be inferred from (7). If the PMOS transistor and the NMOS transistor are well matched, $V_M = V_{DD}/2$. For fast NMOS (lower $V_T$) and slow PMOS (higher $V_T$) transistors $V_M < V_{DD}/2$ and, conversely, for slow NMOS (higher $V_T$) and fast PMOS (lower $V_T$) transistors $V_M > V_{DD}/2$. This is exemplified in Fig. 3.2.2. Assuming that the threshold voltages can vary by ±30mV around the typical (TT) value. In Fig. 3.2.2 the supply voltage is 150mV, FS stands for fast NMOS and slow PMOS transistors, while SF stands for slow NMOS and fast PMOS transistors.

A variation in the process parameters also affects the rise and fall times of the inverter, as equation (16) shows. Variations of an order of magnitude in the NMOS or PMOS drain currents result in rise and fall times that also differ by an order of magnitude. This represents a waste of energy since the maximum operating frequency is mostly determined by the highest sum of the expected fall and rise times. Therefore, proper techniques must be applied in order to compensate, to some extent, for the large variations in the drive currents and, consequently, avoid wasting of energy. Figure 3.2.3 shows the transient simulation of the charge and discharge of a load capacitor, $C_L=50\text{fF}$, driven by an inverter with different NMOS and PMOS drain current capabilities, for a supply voltage of 200 mV. The rise and fall times are clearly very different due to the slow NMOS and fast PMOS transistors.

Expression (1) also shows that a variation in the source-to-body voltage, $V_{SB}$, of the transistor affects the drain current. With a proper body voltage, mismatches in the drive current in the NMOS and PMOS can be reduced regardless of their sizes and technological parameters. Reverse body biasing (RBB) is a technique in which the

![Fig. 3.1: The 2-input NAND gate.](image1)

![Fig. 3.2: NMOS and PMOS drain current.](image2)

![Fig. 3.2.2: Inverter VTC under the influence of a variation in the process parameters.](image3)
body-bias voltage is higher than $V_{DD}$ for the P transistor and lower than GND for the N transistor.

![Fig. 3.2.3.Transient simulation of the charge and discharge of a 50fF load capacitor by an unbalanced CMOS inverter.](image)

Technique is good for leakage current reduction, but has the great inconvenience of the need for bias voltages higher than $V_{DD}$ and lower than GND. Forward body biasing (FBB) is another technique in which the body voltages are between GND and $V_{DD}$. An inverter with body-bias voltages $V_{BN}$ and $V_{BP}$ is shown in Fig. 3.2.4.

![Fig. 3.2.4.Inverter with body bias.](image)

### IV. PROPOSED MODEL

Low power has emerged as a principal theme in today’s electronics industry. The need for low power has caused a major paradigm shift, where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static and Dynamic Power. Static (Leakage) power: includes sub-threshold leakage, drain junction leakage and gate leakage due to tunnelling. Among these, sub-threshold leakage is the most prominent one.

Dynamic power:
Includes charging and discharging (switching) power and short circuit power. In Dynamic power, power consumption due to switching activity is more prominent.

4.1. Optimized circuits

The proposed technique is also applied in this circuit. This circuit is simulated in different 180nm, 130nm 100nm 90nm 70nm 65nm and 45nm technologies.

4.1.1 NAND GATE:
The NAND Technique for low leakage operation of an inverter is depicted in below figure. This inverter though provides significantly leakage power reduction.

![Fig 4.1.1.NAND GATE Inverter of Optimized Circuit1 Design by Tanner Tool.](image)

Above figure shows a NAND Inverter gate. The output is low whenever both input are high, and high otherwise. We can click on the inputs (on the left) to toggle their state. The NAND technique for leakage operation. This inverter though provides significantly leakage technique for leakage power reduction.

4.1.2 NOR GATE:
The conventional NOR gate technique for low leakage operation of an inverter is depicted in below figure. This inverter though provides significantly leakage power reduction.

![Fig 4.1.2.NOR GATE Inverter of Optimized Circuit 2 Design by Tanner Tool](image)
TABLE 1. Compression between NAND GATE Inverter of Optimized Circuit 1 and NOR GATE Inverter of Optimized Circuit 2

<table>
<thead>
<tr>
<th>S.N.</th>
<th>Circuit/Parameter</th>
<th>NAND GATE Inverter of Optimized Circuit 1</th>
<th>NOR GATE Inverter of Optimized Circuit 2</th>
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<td>Technologies.(nm)</td>
<td>Power(watts)</td>
<td>power(watts)</td>
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<td>1.129227e-007</td>
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TABLE 2. CMOS INVERTER of optimized circuit 3

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V. CONCLUSION

In this paper, the basic logic gates aimed at ultra-low voltage operation working principles were summarized. These gates need additional schemes to compensate for Variations in the process parameters, the application of a body-bias voltage being one of the most commonly used compensation methods.

REFERENCES