Design & Analysis of Low Power Full Adder

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Abstract

Addition is one of the fundamental arithmetic operations. It is used in many VLSI systems such as microprocessors and application specific DSP architecture. In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as, subtraction, multiplication, address calculation, etc. The proposed full adder minimizes the power consumption and lesser the delay by SPICE simulation. Due to the minimum time delay of carry out, the adder presented here improves the overall performance for a large scale of multi-bit adder. There are some different types of full adder are taken for comparison with new full adder and found a great improvement in this adder.

Keywords: Spice, Tinor Tool, VLSI etc.

I. INTRODUCTION

Adder core is the most critical building block in microprocessors and digital signal processors. In general, a one-bit full adder core has three inputs and two outputs sum and carry out. The complex arithmetic circuits such as subtraction, multiplication, and division functions usually can be realized by co-operations of multiple adders. An adder performance affects the arithmetic system as a whole. Adder core is the most critical building block in microprocessors and digital signal processors. The complex arithmetic circuits such as subtraction, multiplication, and division functions usually can be realized by co-operations of multiple adders. An adder performance affects the arithmetic system as a whole [1].

In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as, subtraction, multiplication, address calculation etc. The common adders operate on binary numbers. For single bit adders, there are two general types. A half adder has two inputs and two outputs sum and carry. Essentially the output of a half adder is the two-bit arithmetic sum of two one-bit numbers. The other type of single bit adder is the full adder which is like a half adder, but takes an additional input carry. A full adder can be constructed from two half adders.

II. ADDER

A. Half Adder

Half adder is a combinational circuit that performs the addition of two bits; this circuit needs two binary inputs and two binary outputs.

With the help of half adder, we can design circuits that are capable of performing simple addition with the help of logic gates. The truth table and the logic circuit with basic gates of half adder are as follows.

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
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<tbody>
<tr>
<td>A</td>
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Table 1.1: Truth table of Half Adder

Fig 1 Half Adder Circuit

B. Full Adder

A full adder is a logical circuit that performs an addition operation on three binary digits. The full adder produces sum and carry value, which are both binary digits. It can be combined with other full adders or work on its own.

\[ S = (A \ XOR \ B) \ XOR \ Ci \]
\[ Co = (A \ AND \ B) \ OR \ (Ci \ AND \ (A \ XOR \ B)) \]
\[ = (A \ AND \ B) \ OR \ (B \ AND \ Ci) \ OR \ (Ci \ AND \ A) \]

The final OR gate before the carryout output may be replaced by an XOR gate. This is because the only discrepancy between OR and XOR gates occurs when both inputs are 1; for the adder shown here, one can check this is never possible. Using only two types of gates is convenient if one desires to implement the adder directly using common IC chip. The output carry is designated as COUT and the normal output is designated as S. Take a look at the truth-table. From the below truth-table, the full adder logic can be implemented. The output S is an EXOR between the input A and the half-adder SUM output with B and CiN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH.
This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry CIN. A full adder implemented with two half adder is shown below.

![Full Adder Circuit](image)

**Fig 2. Full Adder Circuit**

### Table 2: Truth Table of Full Adder

<table>
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### C. Single Bit & Multi Bit Adder

Though the implementation of larger logic diagrams is possible with the above full adder logic a simpler symbol is mostly used to represent the operation. Given below is a simpler schematic representation of a one-bit full adder.

![Single Bit Adder](image)

**Fig 3: Single Bit Adder**

Full Adder is a combinational circuit that performs the addition of three bits. It consists of three inputs and two outputs, two inputs are the bits to be added, the third input represents the carry formed by cascading two of the 4-bit blocks. The full adder is usually a component in a cascade of adders, which add 8, 16 and binary numbers. The output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The output has a carry 1 if two or three inputs are equal to 1. In a computer, for a multi-bit operation, each bit must be represented by a full adder and must be added simultaneously [13].

![Multi Bit Adder](image)

**Fig 4: Multi Bit Adder**

### D. DESIGN & CHARACTERISATION OF DIGITAL CIRCUITS FOR LOW POWER.

Low power industry is growing at a very rapid rate. One of the factors behind this rapid growth is the handheld devices which operate on battery. The battery technology has not improved as compared to VLSI also if we employ more power to batteries there is a risk of explosion, so we have the only option i.e. to design new low power circuits and design techniques [1] [2].

From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence the lower the impact on global environment, the less the office noise (e.g., due to elimination of a fan from the desktop), and the less stringent the office power delivery or heat removal requirements.

### III. POWER CONSIDERATIONS

Power dissipation in CMOS circuits is caused by three sources:-

- The leakage current which is primarily determined by the fabrication technology consists of reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage.
- The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions.
• The charging and discharging of capacitive loads during logic changes (Dynamic Power Dissipation).
• The dominant source of power dissipation is the charging and discharging of the node capacitances (dynamic power dissipation) and is given by:

\[ P = 0.5 \times C \times V_{dd} \times 2E(sw) \times f_{clk} \]

Where \( C \) is the physical capacitance of the circuit, \( V_{dd} \) is the supply voltage, \( E(sw) \) (referred as the switching activity) is the average number of transitions in the circuit per 1/f_{clk} time, and \( f_{clk} \) is the clock frequency.

There are three degrees of freedom inherent in the low-power design space:

1. Voltage
2. Physical Capacitance (Area)
3. Data Activity (Speed)

Optimizing for power entails an attempt to reduce one or more of these factors. Below is the description of each of these factors and their relative importance, as well as the interactions that complicate the power optimization process.

A. Voltage Vs Area & Delay
Because of its quadratic relationship with power, voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits or techniques, a factor of two reductions in supply voltage yields a factor of four decreases in power consumption. Furthermore, this power reduction is a global effect, experienced not only in one sub-circuit or block of the chip, but throughout the entire chip.

Because of these factors, designers are often willing to sacrifice increased physical capacitance (AREA) or circuit activity (SPEED) for reduced voltage [3]. Another approach is to reduce the supply voltage without loss in throughput is to modify the \( V_t \) of the devices. Reducing the \( V_t \) allows the supply voltage to be scaled down without any loss in speed. The limit of how low the \( V_t \) can go is set by the requirement to set adequate noise margins and control the increase in sub threshold leakage currents; the optimum \( V_t \) must be determined based on the current drives at low supply voltage operation and control of the leakage currents. Since the inverse threshold slope (S) of a MOSFET is invariant with scaling; for every 80-100 mV (based on the operating temperature) reduction in \( V_t \), the standby current will be increased by one order of magnitude. This tends to limit \( V_t \) to about 0.3 V, for room temperature operation of CMOS circuits.

B. Physical capacitance (Area) Vs. Delay
Dynamic power consumption depends linearly on the physical capacitance being switched (charging and discharging). So, in addition to operating at low voltages, minimizing capacitances offers another aspect for minimizing power consumption. Power dissipation is dependent on the physical capacitances seen by individual gates in the circuit. Capacitances can be kept at a minimum by using less logic, smaller devices, fewer and shorter wires. Techniques for reducing the active area include resource sharing, logic minimization and gate sizing [4]. As with voltage, we are not free to optimize capacitance independently. For example, reducing device sizes reduces physical capacitance, but it also reduces the current drive of the transistors making the circuit operate more slowly (increased delay). This loss in performance might prevent us from lowering \( V_{dd} \) [5] [6].

C. Switching Activity (Speed) Vs. Area

IV. PROPOSED FULL ADDER
The architecture of the new full adder is directly realized by two modules. Figure 26 shows the conceptual diagram [7].

• Module 1 implements three-input XOR function based on equation of SUM.
• Module 2 implements the function of equation of CARRY.

Fig 5: Conceptual Diagram of Full Adder

The architecture of the new full adder is directly realized by two modules. Figure 5 shows the conceptual diagram. Module 1 implements three-input XOR function based on SUM equation and module 2 implements the function of CARRY [8].

The full adder composed of pass transistor logic (PTL) [11] [12 and static CMOS logic is named here as ‘Hybrid full adder’. The novel hybrid full adder shows that due to the minimum time delay of carry out, the adder core greatly improves the overall performance for a large scale of multi-bit adder.

The function of a full adder can be expressed as

\[ S = (A \times \text{XOR} \ B) \times \text{XOR} \ C_i \]

\[ C_o = AB + (A+B) \times C_i \]

A. Three Input XOR Circuitry
Conventionally, three-input XOR function is often realized by cascading two two-input XOR gates [9] [10]. Figure 27 shows a direct design of a three-input
CMOS XOR circuit. The advantages of Fig. 27 are simple structure and with output driving capability. However, the power consumption is not small enough. A new version of Fig. 27 is proposed as shown in Fig. 28. The output inverter is rearranged at Ci input terminal. Although it is merely simple modification, the power consumption and speed are greatly improved. SPICE simulation normalized results based on the simulation values for both reference and proposed three-input XOR circuitries. Obviously, the performance of the new XOR circuit (NEW 3-XOR) improves in power consumption and in delay time. It is obvious that we if decrease the clock frequency (SPEED), what we can do is; to gate that set of input which is not contributing towards the output, but again with the cost of increased area [10].

Fig 6: Three Input CMOS XOR Circuit

Fig 7: Modified Three Input CMOS XOR Circuit

B. Carry-out Module
The mirror type circuit shown in Fig. 29 realizes the carry out function. The PMOS tree mirrors to NMOS tree to simplify the chip layout consideration. The circuit is adopted as module 2 of the new full adder.

Fig 8: Modified Carry-out Module

A proposed full adder circuit with modified carry-out is shown in fig. 9. The ‘Sum’ module is in pass-transistor logic style while the ‘Carry out’ module is in mirror type static CMOS logic. ‘Sum’ and ‘Carry-out’ modules need 12 transistors respectively. The total transistor count of the new full adder is thus 24.

Fig 9: Proposed Full Adder Circuit.

C. Circuit Description
In this proposed adder the circuit is a combination of two small circuits one is sum part and another is carryout part. The sum module is basically a three input CMOS XOR circuit and the carry module forms a tree of PMOS (p-type metal oxide semiconductor) and NMOS (n-type metal oxide semiconductor). In sum module the numbers of transistor used are 12 in which 6 PMOS (p-type metal oxide semiconductor) and 6 NMOS (n-type metal oxide semiconductor) are used. The carry module there is also the numbers of transistor used are 12 in which 6 PMOS (p-type metal oxide semiconductor) and 6 NMOS (n-type metal oxide semiconductor) are used. So there are total 24 transistor are used. The circuit is shown in figure 10 [14] [15].

Fig 10: Schematic Circuit of Proposed Full Adder

In this proposed full adder circuit 12 p- type metal oxide semiconductor (PMOS) and 12 n- type metal oxide semiconductor (NMOS) used. The W/L ratio (W/L=10), M=1(Multiplicity factor which means
number of MOSFET used in parallel) and \( NF = 1 \) (noise factor which also called as number of device fingers) of PMOS and NMOS in this full adder circuit with 5v supply. We give a pulse with 1ns rise and 1ns delay time and with 25ns pulse width 50ns per cycle as input (i/p) shown in figure and find out the result with minimum delay as output (o/p). The waveforms are shown in figure 11.

The new full adder is designed and the transient analysis is done. Here are some different types of full adders are taken for comparison with the proposed full adder. On the basis of comparative analysis the power consumption of the proposed CMOS full adder is reduced because the number of transistors used is reduced. There is also an improvement in speed because the delay in propagation of carry out signal is reduced according to the transient analysis in given simulation time. Linearity improvement is also an important factor in this analysis. So it is proved that the new full adder is more efficient for embedded system.

![Waveform of Proposed Full Adder](image)

Fig 10: Waveform of Proposed Full Adder

V. CONCLUSION & FUTURE SCOPE OF WORK

The characteristics of the proposed full adder circuit are compared against five previous designs for average delay time and power consumption. The compared results show that the performance of the proposed design is superior to other reference designs. By SPICE simulation, an outstanding improvement of the circuit than prior literature in power consumption and in time delay of Co. The properties of the fastest response of Co and the minimum power consumption per cell are useful for a large scale of adder realization. The experiment shows that the proposed adder core is valid and effective for embedded system.

In future we can improve the performance of this full adder in terms of delay, linearity and speed. We can also improve other parameters of this proposed full adder.

References


