Design of CMOS Inverter Using Different Aspect Ratios

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ABSTRACT
The aim of this paper is to show the effect of W/L ratio parameters of CMOS, which characterized the CMOS structure. It is also analysis the current value, threshold voltage value and other related parameters of CMOS inverter. MOSFET device is the 4 terminal devices GATE, DRAIN, SOURCE AND BODY (substrate). W/L is the most important factor of CMOS. Hence considering we can change the value of W/L of CMOS and then measure the physical parameters to reach the accepted goal using Microwind 3.1 software.

Key words: CMOS parameters, threshold voltage, W/L ratio.

I. INTRODUCTION
CMOS is by far the most popular technology for the implementation of digital systems. The small size, ease of fabrication, and low power dissipation of MOSFETs enable extremely high levels of integration of both logic and memory circuit’s. Digital IC Technologies and Logic-Circuit Families. CMOS: CMOS technology is, by a large margin, the most dominant of all the IC technologies available for digital-circuit design. These are a number of reasons for this development, the most important of which is the much lower power dissipation of CMOS circuits. Generally all parameters of CMOS are depending on the w/l ratio. Analysis the parameters of CMOS after changing in the w/l ratio. CMOS parameters change when w/l ratio is followed.

1. w = 1 µm, & L = 1 µm
2. w = 0.5 µm & L = 1 µm
3. w = 1 µm & L = 0.5 µm
4. w = 0.5 µm & L = 0.2 µm

CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuits on a chop than is possible with bipolar circuits. The high input impedance of the MOS transistor allows the designer to use charge storage as a means for the temporary storage of information in both logic and memory circuits.

II. NMOS LOGIC DESIGN & NMOS INVERTER CIRCUIT
MOS transistors (both PMOS and NMOS) can be combined with resistive loads to create single channel logic gates.

The circuit designer is limited to altering circuit topology and the width-to-length (W/L) ratio since the other factors are dependent upon processing parameters. Resistive load inverter takes up too much area for and IC design. The saturated load configuration is the simplest design, but \( V_H \) never reaches \( V_{dd} \), and it has a slow switching speed. The linear load inverter fixes the speed and logic level issues, but it requires an additional power supply for the load gate. The depletion-mode NMOS load requires the most processing steps, but needs small area to achieve the high speed, \( V_H = V_{dd} \), and best combination of noise margins. The Pseudo NMOS inverter offers the best speed with the lowest area.

III. CMOS INVERTER
CMOS transistors use all three bias states described here: OFF-state, saturated-state, and the linear -state (ohmic, non-saturated). We will next look at curves illustrating MOS transistor parameters, and learn the analytical equations that predict and analyze transistor behavior. It is important to work through all examples and exercises. It is instructive to return to this transistor description after acquiring skill in transistor circuit analysis.

CMOS inverter is the combination network of pull-up-network and pull-down-network. Pull-up-network is known as load part, where as we can use totally PMOS. The PMOS pull-up-network, on other hand, must be the dual network of the n-net. This means that all the parallel connection in the NMOS pull-down-network

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will correspond to a series connection in the PMOS pull-up-network, and all the series connection in the NMOS pull-down-network will correspond to a parallel connection in the PMOS pull-up-network.

![CMOS inverter circuit](image1)

**IV. CHARACTERISTICS OF CMOS INVERTER**

We know that an inverter can act as an inverter provides maximum output on minimum input. A CMOS inverter performs this operation in different modes as CUTT OFF, SATURATION, LINEAR. CMOS provide maximum output on minimum input and minimum output on max input. CMOS operates in those modes, they are followed...

![CMOS inverter characteristics curve](image2)

V. MOSFET PARAMETERS
- $i_p$ – Drain current
- $V_{TP}, V_{TN}$ – Threshold voltage ($V_{TH}$)
- $v_{DS}$ – Drain to source voltage
- $v_{GS}$ – Gate to source voltage
- $v_B$ – Bulk voltage

VI. OXIDE CAPACITANCE
- $C_{ox} = E_{OX} / T_{OX}$
- $E_{OX} = 3.9 \varepsilon_0$
- $\varepsilon_0 = 8.85 \times 10^{-14} \text{F/CM}$

VII. PARAMETER DEFINITIONS
- $\mu_{n,p}$ – Electron or hole mobility
- $\varepsilon_{ox}$ – Permittivity of oxide
- $t_{ox}$ – Oxide thickness
- (W/L) – Aspect ratio

$$v_{GS} < V_{TH} \quad \Rightarrow \quad i_p = 0$$

$$v_{ds} < (v_{gs} - V_{TH}) \quad \Rightarrow \quad i_p = k_p \left( \frac{W}{L} \right) (v_{gs} - V_{TH}) v_{ds} - \frac{1}{2} v_{ds}^2$$

$$v_{ds} \geq (v_{gs} - V_{TH}) \quad \Rightarrow \quad i_p = 2k_n \left( \frac{W}{L} \right) (v_{gs} - V_{TH})^2$$

VIII. DURING CHANGE THE W/L RATIO

W/L ratio is the most important parameter of the inverter. Inverter channel & flow of current and all parameters of CMOS /NMOS are effected. In this paper we have study the all parameters of CMOS during changing in the w/l ratio. Change the w/l ratio as half, double and same width or as requirement of operation. The following layout of a MOSFET has given L=4 λ and W=8 λ. Use the EE143 layout graph paper to layout a minimum-size transistor. Label the design rules you used.

![CMOS inverter layout](image3)
[Note: An integrated circuit usually has MOSFETs with different L and W values. To reduce the contact resistance, it is desirable to maximize the metal contact area to the source/drain regions. To optimize optical lithography and reactive ion etching steps, it is preferable to place several identical-size contact holes within the S/D regions instead of a single large one.]

IX. CHANNEL LENGTH MODULATION

MOS Transistor: Deviations From Ideal

Channel Length Modulation Effect

But the fraction of the channel that is pinched off depends linearly on \( V_{GS} \), because the voltage across the pinch-off region is \( (V_{GS} - V_{TO}) \).

\[
\frac{\Delta L}{L} = \lambda V_{GS}
\]

where \( \lambda \) is known as the Channel-Length Modulation parameter and is typically:

\[
0.001 \text{ V}^4 < \lambda < 0.1 \text{ V}^{-1}
\]

\[
I_D = I_{Dsat} = \frac{Z \mu_n C_m}{2L} \left[ (V_{GS} - V_{TH})^2 \right] (1 + \lambda V_{GS}) \quad V_{GS} \leq V_{TH}
\]

X. TRANSISTOR SIZING

The inverter threshold voltage \( v_{th} \) was identified as one of the most important parameters that characterize the steady-state I/O behavior of the CMOS inverter circuit. The CMOS inverter can, by virtue of its complementary push-pull operating mode, provide a full output voltage swing b/w 0 and Vdd, and therefore, the noise margins are relatively wide. Proper design of W/L ratio is very important to find the current driving capability of gate in both directions. Reorganizing yields

\[
\sqrt{1/k_r} = \frac{(v_{th} - v_{to, n})}{(v_{dd} + v_{to,p} - v_{th})}
\]

(1)

Now solve for \( k_r \) that is required to achieving the given \( V_{th} \).

\[
k_r = \frac{V_{dd} + v_{to,p}}{v_{th} - v_{to,n}} \times \left( \frac{1}{2} \right)
\]

(2)

Recall that the switching threshold voltage of an ideal inverter is defined as,

\[
V_{th, ideal} = \frac{1}{2} V_{dd}
\]

(3)

Substituting (3) in (2) gives

\[
\frac{(V_{DD} + v_{to,p})^2}{(0.5V_{dd} - v_{to,n})^2}
\]

(4)

For a near-ideal CMOS VTC that statics the (3).since the operation of the NMOS & the PMOS transistor of the CMOS INVERTER are fully complement.

\[
\frac{(V_{DD} + v_{to,p})^2}{(0.5V_{dd} - v_{to,n})^2} = \frac{(V_{DD} + v_{to,p})^2}{(0.5V_{dd} - v_{to,n})^2}
\]

(5)

Hence,

\[
\frac{(W/L)_n}{(W/L)_p} = 2.5(W/L)_n
\]

Example

Calculate \( I_D \) and \( V_{DS} \) if \( K_n = 100 \mu A/V^2 \), \( V_m = 0.6 \) V, and \( W/L = 3 \) for transistor M1. The bias state of M1 is not known so we must initially assume one of the two states, then solve for bias voltages and check for consistency against that transistor bias condition. Initially, assume that the transistor is in the saturated state so that

When \( W/L \) ratio is 3, we can say that \( w=6 \mu m \) and \( L=2\mu m \) then \( W/L=3 \)

\[
I_D = \mu_n C_{ox}/2T_{ox} \times W/L \times (VGS - V_m)^2 = KnW/L (VGS - V_m)^2
\]

= (100 \mu A) (3) (1.5 - 0.6)^2

= 243 \mu A

Using Kirchhoff's Voltage Law (KVL)

\[
V_{DS} = V_{DD} - IDR
\]

= 5 - (243 \mu A) (15 k\Omega)

= 1.355 V
We assumed that the transistor was in saturation, so we must check the result to see if that is true. For saturation
\[ V_{GS} < V_{DS} + V_{tn} \]
1.5 V < 1.355V + 0.6V
So the transistor is in saturation, and our assumption and answers are correct.

(a) **changing the W/L ratio:** w=1µm and l=1µm, so w/l=1
\[
I_d = \frac{\mu_n \cdot C_{ox}}{2 \cdot T_{ox}} \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2 = Kn \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2
\]
= (100 µA) (1) (1.5 - 0.6)^2
= 81 µA
Using Kirchhoff's Voltage Law (KVL)
\[ V_{DS} = V_{DD} - I_D \cdot R \]
= 5 - (81µA) (15 kΩ)
= 3.785 V

(b) **changing the W/L ratio:** w=1µm and l=0.5µm, so w/l=2
\[
I_d = \frac{\mu_n \cdot C_{ox}}{2 \cdot T_{ox}} \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2 = Kn \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2
\]
= (100 µA) (2) (1.5 - 0.6)^2
= 162 µA
Using Kirchhoff's Voltage Law (KVL)
\[ V_{DS} = V_{DD} - I_D \cdot R \]
= 5 - (162µA) (15 kΩ)
= 2.57 V

(c) **changing the W/L ratio:** w=0.5µm and l=1µm, so w/l=0.5
\[
I_d = \frac{\mu_n \cdot C_{ox}}{2 \cdot T_{ox}} \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2 = Kn \cdot \frac{W}{L} \cdot (V_{GS} - V_{tn})^2
\]
= (100 µA) (0.5) (1.5 - 0.6)^2
= 40.5 µA
Using Kirchhoff's Voltage Law (KVL)
\[ V_{DS} = V_{DD} - I_D \cdot R \]
= 5 - (40.5µA) (15 kΩ)
= 4.3925 V

<table>
<thead>
<tr>
<th>Operation</th>
<th>( V_{ds} ) (( v_{out} ))</th>
<th>( I_d ) (drain current)</th>
</tr>
</thead>
<tbody>
<tr>
<td>w=0.5µm and l=1µm, so w/l=0.5</td>
<td>4.3925V</td>
<td>40.5 µA</td>
</tr>
<tr>
<td>w=1µm and l=1µm, so w/l=1</td>
<td>3.785V</td>
<td>81µA</td>
</tr>
<tr>
<td>w=1µm and l=0.5µm, so w/l=2</td>
<td>2.57V</td>
<td>162 µA</td>
</tr>
<tr>
<td>w=6 µm and L=2µm then W/L=3</td>
<td>1.355V</td>
<td>243µA</td>
</tr>
</tbody>
</table>

Figure 5: CMOS inverter with w=1µm and L=1µm

2. When, w=1µm and l= 0.5µm, so w/l=2
3. $W=0.5\mu M$ AND $L=1\mu M$, SO $W/L=0.5$

4. VALUES OF $W/L$ ARE $W=6\mu M$ AND $L=2\mu M$ .... (INTRINSIC TYPE CMOS)
XI. CONCLUSION

Let’s we have to study the effective parameter of CMOS during changing the W/L ratio. W/L is the most effective parameter, which is the ratio of width/length of the NMOS or PMOS device. When we change (increase) the w/l ratio then output voltage ($v_{out}$) is decrease as well as drain current ($I_d$) is increase or Visa - versa.

REFERENCES